Fermi National Accelerator Laboratory

TM-588
0880.000

June 1975

Auxiliary/Master Microprocessor CAMAC Crate Controller

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Summary

Sophisticated applications requiring "local intelligence" in a CAMAC crate lead to the development of an Auxiliary/Master Microprocessor CAMAC Crate Controller for the Fermilab experimental beam line serial CAMAC control system.

Introduction

In early 1972 Fermilab commissioned its serial CAMAC control system for use in the three experimental areas.[1] The first approach for a serial system was to use a serial driver connected through repeaters to several branch drivers controlling up to seven Type A crate controllers each. Data handling requirements lead to the replacement of serial branch drivers by an in-house designed CAMAC Serial Crate Controller with block transfer capabilities.[2] As the system developed, experimenters and operators requested more and more complex data gathering and handling operations from the system.[3] Input and output block transfer operations were increased in an effort to lessen the burden on the CPU of the system computer. Crate to multi-crate block transfers were provided for graphics and sophisticated console requirements. It soon became evident that "local intelligence" in a CAMAC crate was necessary. Applications such as closed loop control and status and alarm checking of a few devices could more easily be handled by an intelligent auxiliary crate controller (ACC). As the ACC was being developed, new applications emerged, some requiring an auxiliary controller and some requiring a stand-alone or master crate controller (MCC). Controlling the focusing horn in the Neutrino Experimental Area and controlling an entire experiment in the Internal Target Area of the Main Accelerator were two additional applications for the newly named Auxiliary/Master Crate Controller (A/MCC).[4]

Microprocessor Hardware

The auxiliary/master crate controller contains a Motorola 6800 microprocessor, 1-7/8K bytes of Motorola 6810 RAM and up to 8K bytes of Intel 2708 PROM memory. The microprocessor cycle time is presently 1.25 microseconds for internal memory and can be phase-modulated to 1.75 microseconds for slower external memory or peripheral addressing.

Time Sharing the Dataway

When used as an auxiliary crate controller, the A/MCC time shares the dataway with both Serial Crate Controller (SCC) block-transfer and normal-transfer generated dataway cycles. At all times other than during dataway cycles, the A/MCC can be using the dataway for memory expansion and peripheral addressing.

Memory Expansion

Since the microprocessor is a byte (eight bit) oriented machine with capability of addressing 65K bytes of memory, twenty-four lines in addition to a few control lines are required to extend memory. By lowering the dataway busy signal while addressing memory, the A/MCC is able to use the 24 dataway read lines for address and data along with four other bussed dataway lines to extend memory. The only requirement is that the microprocessor be held in an inactive state during SCC or A/MCC generated dataway cycles. This feature allows the extension of memory and peripheral addressing through the dataway to CAMAC modules without the need of external cabling.

Time sharing the dataway between SCC programmed and block transfer generated dataway cycles and A/MCC operations still allows a 99% microprocessor CPU busy time.

Peripheral Addressing

The 6800 microprocessor allows for 256 bytes of directly addressable memory, 128 of these bytes are used for addressing peripherals in addition to registers internal to the A/MCC. These latter registers require 32 of the 128 addresses, leaving the A/MCC capable of addressing up to 96 peripheral devices. Using directly addressable locations for the most frequently used memory locations allows for more efficient operation of the A/MCC by saving both program bytes and MPU cycle times.

Interrupt Handling

The microprocessor has one non-maskable and one maskable vectored interrupt. The non-maskable interrupt has three sublevels of vectored interrupts, one each for communications from an SCC to the A/MCC, block transfer operations and, if used, a 60Hz real time clock. The maskable interrupt has 8 sublevels of vectored interrupts. Any combination of four front panel or eight LAM signal interrupts, or a hardware timeout can be wired to the eight maskable interrupts. Sublevels of vectored interrupts are derived by latching and priority encoding the interrupts. An add instruction to the prioritized interrupt is then used to obtain a vector for servicing the interrupt. This hardware/software tradeoff provides relatively fast servicing of interrupts without a large amount of hardware.

Memory Allocation

The basic A/MCC contains 1-7/8K bytes of RAM and up to 8K bytes of PROM memory in addition to 32 bytes of internally addressed registers. The table below specified memory allocation for these locations in addition to that for the remaining 55K (65-[8 + 2]) bytes of memory.

Addresses	Description	Bytes
0000-007F	Directly Addressable A/MCC Internal RAM Memory	1/8K
0080-009F	Directly Addressable A/MCC Internal Register	32
00A0-00FF	Peripheral Addresses	96
0100-07FF	A/MCC Internal RAM Memory	1-3/4K
0800-DFFF	External PROM, ROM, or RAM Memory	≈55K
E000-FFFF	A/MCC Internal PROM Memory	≤8K

A/MCC Construction

The A/MCC consists of two modules, one single-width and one double-width. The double-width module contains the necessary crate controller hardware, i.e., read/write registers, station number registers, dataway cycle timing generator, etc., in addition to hardware providing input and output block transfer capabilities through the SCC. When the A/MCC is functioning as an auxiliary controller, the single width module contains the microprocessor, RAM, PROM, MPU clock and the timing and logic circuitry required for interleaving A/MCC and SCC dataway cycles and

extending memory via dataway lines. A second single-width module may be used in place of the module described above when the A/MCC is used as a master controller. This module excludes the timing and logic circuitry used to interleave dataway cycles but contains circuitry for performing cycle stealing DMA transfers. Both single modules may contain drivers and receivers for extending microprocessor control to additional local crates.

Auxiliary or Master Crate Controller

The A/MCC can reside in any group of three slots while functioning as a master crate controller and in any three slots excluding the three right most slots while functining as an auxiliary controller to the SCC.

Changing from an auxiliary to a master crate controller or vice-versa is easily accomplished by the insertion or extraction of six actual dual-in-line packages. The six packages, when inserted, connect the dataway LAM and station number lines to the A/MCC.

Access to Station Number (N) and LAM (L) Lines

A rear I/O connector and harness from the A/MCC double-width module to the control station of the crate allows the A/MCC to access station number and LAM lines when not occupying the three rightmost slots.

SCC Auxiliary Controller Lockout Signals

Five signals are required from the SCC to allow the A/MCC, functioning as an auxiliary controller, to time share the dataway. These five signals tell the A/MCC when a dataway cycle generated by the SCC is eminent. Since the SCC is the master controller, the A/MCC must relinquish the use of the dataway until that dataway cycle is complete. The lockout signals are transmitted to the A/MCC via the five patch pins of the dataway. The A/MCC is held in an inhibited state by phase modulating and statisizing the microprocessor clock for a period not exceeding 2.75 microseconds.

Communications Between Auxiliary A/MCC Controller and SCC

Whenever the A/MCC is addressed by the SCC, the function code and sub-address lines are stored in internal A/MCC registers along with the write data lines for a write function code. The latching of data triggers the microprocessor's non-maskable interrupt initiating an application or "type code" program predefined via A/MCC software. Thus, the F, A, and W lines define an extremely large set of "type code" operations for various A/MCC applications.

The A/MCC communicates with the SCC via four 24-bit SCC readable registers. Four flip-flops, one for each register, are used to indicate to the A/MCC that the registers have been read by the SCC. For example, a flip-flop is set when its corresponding register is loaded and cleared when that register is read by the SCC.

Remote Device Control and Monitoring

The serial system at Fermilab allows for easy communication between experimenter's,computers, and the main system computer by the use of two bi-directional buffered memory modules.[3] By using the same system software and making the A/MCC respond identically to one of these modules the A/MCC can control and/or monitor any device in any crate in the serial system.

Additional Features

Software/hardware tradeoffs in any system are always difficult to evaluate. To ease the software burden, a 60Hz real time clock and a hardware timeout, each driving interrupts,have been incorporated into the A/MCC. Some additional features are described below.

I/O Block Transfer Capabilities

Input block transfers from an ACC are accommodated via circuitry and software which sequentially loads one of the 24-bit registers, halts the microprocessor, waits for a SCC generated block transfer read operation. This operation then takes the MPU out of the halt state and the process is repeated until the transfer is completed.

Block transfer data operations to the ACC are accomplished in much the same manner, except data enters the controller via a special front panel input port.

Local Multi-Crate Expansion

For systems requiring locally more than one crate of hardware, the A/MCC's single-width module can interface to a group of "daisy-chained" crate controller interface modules. These modules are used to control an A/MCC double-width module residing in each of these "daisy-chained" crates.

Maintenance and Testing

The front panel indicators, test points, and switches allow for simple program testing and maintenance. A program may be single-stepped or restarted periodically via front panel controls.

A/MCC Applications[4]

Figures 1 and 2 show typical applications for the A/MCC. Figure 1 depicts the hardware necessary for operating an experiment without the aid of a large or mini-computer. Figure 2 shows a more complex system which is interconnected via an ACC to a large serial CAMAC system. This application also uses the ACC to drive two additional CAMAC crates via interface modules and double-width modules of an A/MCC.

Future Developments

One of the main concerns with a device such as the A/MCC is how to initially test the system software and, if changes are required, how to easily make those changes. A CAMAC module and accompanying software will be developed to program PROM's for the A/MCC. Teletype, digital cassette, and paper tape reader interfaces will need developing to make initial software checking simpler. For large temporary bulk storage, a module containing 4-8K of RAM memory will be developed.

Conclusions

Microprocessors and intelligent crate controllers have indeed opened another phase of developments in the expanding world of CAMAC.

References:

1. L. J. Hepinstahl, et al., CAMAC Experimental Beam Line Control System, 1973 Particle Accelerator Conference.
2. E. J. Barsotti, CAMAC Serial Crate Controller, CAMAC Bulletin No. 6, March 1973.
3. E. J. Barsotti, Operational Aspects of a Serial CAMAC Control System, Nuclear Science Symposium, 1973
4. E. J. Barsotti, Auxiliary/Master Microprocessor CAMAC Crate Controller Applications, submitted paper, 1975 Nuclear Science Symposium.

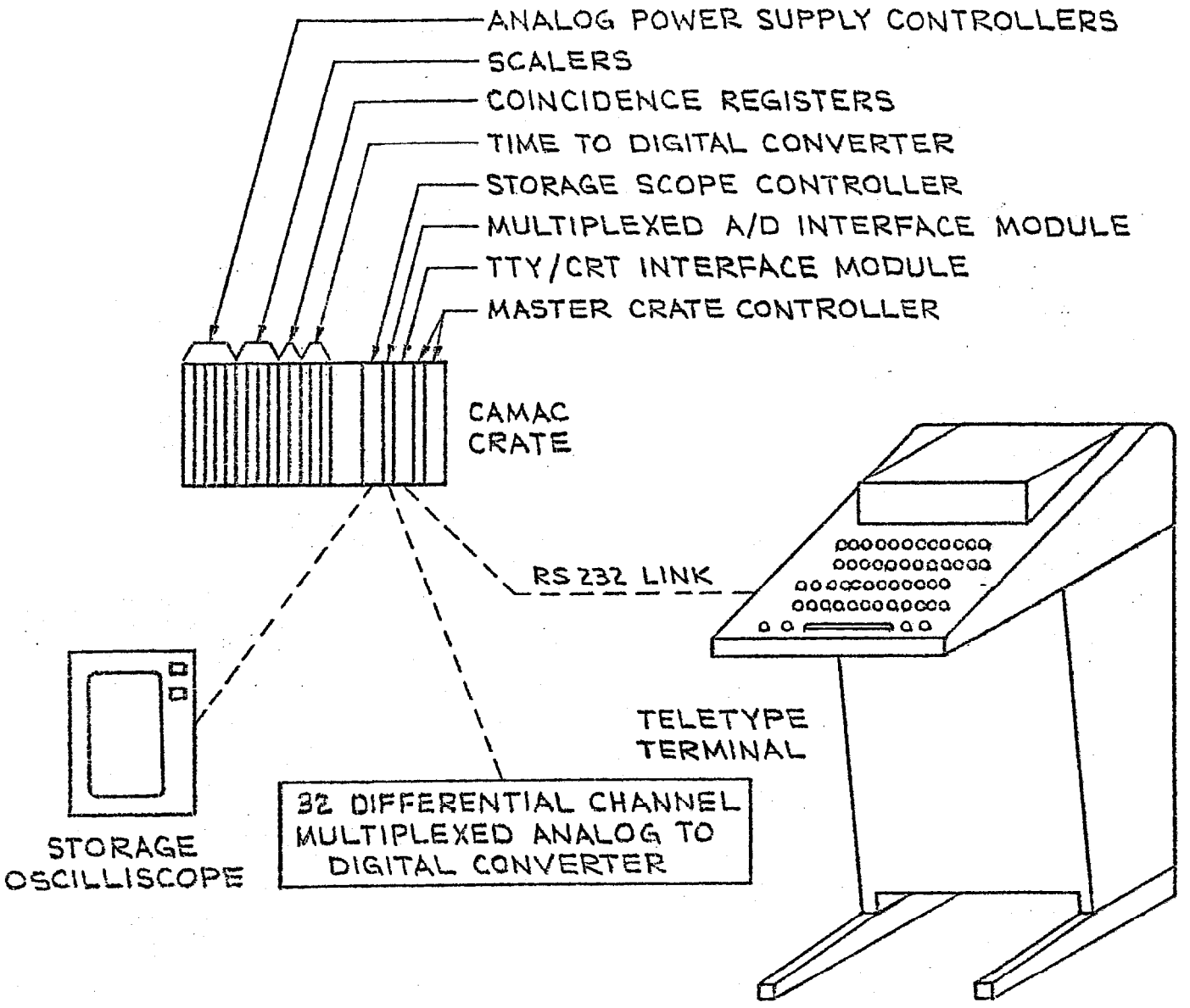

FIGURE 1

MASTER CRATE CONTROLLER APPLICATION
STAND ALONE EXPERIMENT

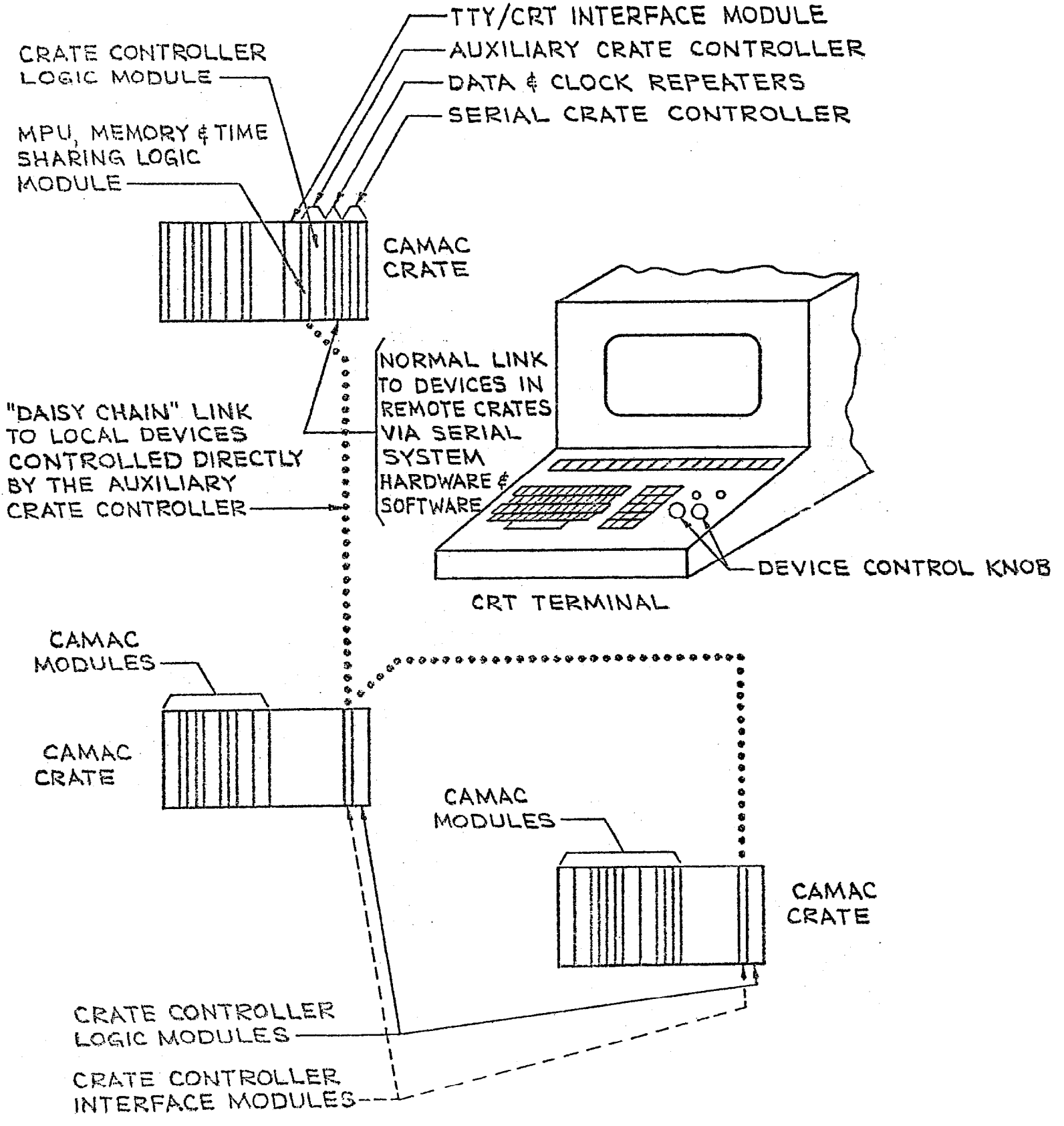

FIGURE 2

AUXILIARY CRATE CONTROLLER APPLICATION
LOCALLY AND REMOTELY MICROPROCESSOR-CONTROLLED SYSTEM